Claims 1 and 2 have been editorially revised to be more consistent in phraseology.

Claims 1 and 3 were rejected as unpatentable over Sano in view of McCaslin et al. The claimed invention compares two signals by generating statistical data from binary words based upon comparisons of the input signals. Accumulated words are compared with a threshold. Neither patent remotely suggests the invention.

In FIG. 5, the Sano patent discloses adjusting the gain of amplifier 54 in accordance with whether or not a transmitted signal is greater than a received signal. In other words, the decision whether to transmit or receive is based upon a single comparison.

The selection from the McCaslin et al. patent relied on by the Examiner relates to FIG. 3 of the patent, an "utterance" detector. As expressly disclosed in column 8, lines 34ff, detector 80 is a far end detector and there is also a near end detector of similar construction. In other words, FIG. 3 relates to detecting speech, not to comparing the microphone signal with the line input signal to determine whether to transmit or receive. It is respectfully submitted that there is no basis for the combination of the McCaslin et al. patent with the Sano patent. The Examiner's comments about noise (1) appear to relate to FIG. 2 of the McCaslin et al. patent but do not relate to FIG. 3 and (2) completely ignore the explanation given in the McCaslin et al. patent of avoiding the problem of arbitrarily decreasing the SERLE value (column 7, lines 43ff) which takes place "at the onset of each utterance."

The McCaslin et al. patent defines an utterance as "a transient increase in ... signal power." It is respectfully submitted that this completely teaches away from the claimed invention in which counts are analyzed to determine whether to transmit or receive. Such momentary increase in signal power would simply be seen as a signal exceeding a threshold for a brief time. The magnitude of the transient would not be detected because magnitude is not measured in the invention. The invention operates in a fundamentally different way from the prior art, including the McCaslin et al. patent. Thus, even if the disclosure of the McCaslin et al. patent could somehow be combined with the disclosure of the Sano patent, the result would not be applicants' invention.

It is noted that the Examiner has not specifically said how to modify the apparatus disclosed in the Sano patent in accordance with the teachings of the McCaslin et al. patent. "Applying" a counter is not understood.

The additional prior art cited in rejecting claimed 2, 4, 5, and 6 moves yet further afield. The prior art cited does not operate in the manner claimed nor overcome the deficiencies noted above with the Sano patent and the McCaslin et al. patent.

The Miller patent is woefully mischaracterized as teaching that one can use "one or more accumulators ... to produce binary signals." What the cited portion of the Miller patent does disclose is the following.

> It is helpful to note at this point that, besides accumulator 3206, there is a substantially identical accumulator (not shown) that is utilized whenever multitone output functions are requested. The second sine/cosine generator, based on a second frequency word (f.sub.w2), is nested within the SINCOS subroutine and is designated by SINCOS2 entry point in FIG. 97.

A "multitone output function" is an **analog** signal. The Miller patent is talking about using a second accumulator to generate DTMF signals. A DTMF signal includes two tones.

The Examiner's assertion also has a tautological element in that digital components, such as accumulators, produce binary, i.e., digital, signals. Even as a tautology, the Examiner's comment is not an accurate summary of the cited portion of the Miller patent.

The Examiner further asserts that "multiple accumulators are needed whenever multiple indicative output signals are requested." This comment does not appear to relate in any way to the Miller patent or to applicants' invention and, on its own, is not understood. Claims 4–6 do not recite accumulators producing output signals, indicative (of what?) or otherwise.

Claims 7 and 8 were rejected as unpatentable over Miller in view of Reesor et al. The Miller patent is a "jumbo" patent whose relevance is not at all apparent. If it were cited for the disclosure of a counter, surely less voluminous patents are available for the purpose. The citation appears to obfuscate rather than enlighten.

Accumulator 4160 is not in FIG. 96 as alleged. Accumulator 4160 was found in FIG. 115.

FIG. 116 is a flow chart. Multiplexers 3501 and 3506 do not appear in the figure; nor does any sort of "boundary control ... having counters and logic."

The Examiner's reference to column 42, lines 39–61, appears to be in error. The cited text refers to measurement processor 3500, multiplexers, quadrature signals and appears to relate to FIG. 17, not FIG. 96 (a circuit) nor FIG. 116 (a flow chart) as alleged.

The Examiner's reference to column 44, line 21, through column 45, line 13, appears to be in error. The text relates to generating a cosine function at various frequencies.

The Examiner's reference to column 48, line 22, through column 49, line 12, appears to be in error. The text covers several topics, e.g. anti-aliasing and synchronous demodulation, none of which relates to "boundary control ... having counters and logic."

The Examiner's reference to column 49, lines 33–68, appears to be in error. The text covers two topics, parallel processing and timing, neither of which relates to "boundary control ... having counters and logic."

The Examiner's reference to column 96, line 49, through column 97, line 4, appears to be in error. The text relates to memory allocation for frequency data, which does not relate to "boundary control ... having counters and logic."

The Examiner's reference to column 97, lines 35–42, appears to be in error. The cited text reads as follows.

> It is helpful to note at this point that, besides accumulator 3206, there is a substantially identical accumulator (not shown) that is utilized whenever multitone output functions are requested. The second sine/cosine generator, based on a second frequency word (f_{w2}), is nested within the SINCOS subroutine and is designated by SINCOS2 entry point in FIG. 97.

The text does not relate to "boundary control ... having counters and logic."

The Examiner's reference to column 100, lines 6–27, is as inapposite as the previous reference.

The Examiner's reference to column 105, lines 19–32, appears to be in error. The cited text reads as follows.

> The signals on leads 34001 and 34003 serve as inputs to measurement processor 3500, as depicted in FIG. 23. The AC signal on lead 34001 is split into three paths. One path directly connects to port 1 of the 7-1 MUX in the upper-half of multiplexer 3501. The second path is one input to multiplier 3701 and the third path drives an input to multiplier 3702. The other inputs to multipliers 3701 and 3702 are the TIP(I) and TIP(Q) signals on leads 32007 and 32006, respectively. The operation of multiplier 3701, which is four-quadrant type AD 534 supplied by Analog Devices, is exemplary of the operation of both multipliers 3701 and 3702 and is now considered.

The text does not relate to "boundary control ... having counters and logic."

The Examiner's reference to column 106, lines 1–52, is as inapposite as the previous reference.

The Examiner's reference to column 118, lines 3–17, could be justified on the basis that the text discloses that a register may generate a carry, which is arguably an overflow although overflow and carry are not the same. The Miller patent teaches adding a register to store carries, which is antithetical to (teaches away from) the claimed invention, which *prevents* overflow or underflow in a unique way. Again, why cite a jumbo patent for such an elementary idea as producing a carry?

The Examiner's reference to the Abstract of the Miller patent is also inapposite.

It is therefore respectfully submitted that the Examiner's comments are not supported by the disclosure of the Miller patent.

In discussing the patent to Reesor et al., the Examiner notes that overflow is inherent in an accumulator. First, this is not necessary for the rejection. Second, it is not accurate. Accumulators can be made to behave anyway one wishes. If one permits overflow, then it can happen. If not, it cannot happen. It is not inherent.

The Examiner's assertion that "digital switching network 25 effectively multiplexes the digital signal processor 14 between a plurality of local loudspeaking telephones and outside lines" is vague, tentative, and has nothing to do with claim language.

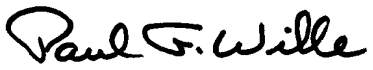
FIG. 5 of the Reesor et al. patent discloses the details of gain control circuit 16A, which details include logic for preventing roll-over or roll-under. Thus, the patent discloses the preamble of claim 7. The remainder of claims 7 and 8 are not

disclosed. The Examiner's comment about digital switching network 25 (FIG. 1C) is obviously not related to the patent because, even if network 25 were a multiplexer as alleged, it is not connected to the logic within block 16A; see FIG. 1C. The inputs to block 16A are coupled to the outputs of DSP 14. Line 15 is disclosed as a unidirectional data line connected as an input to network 25.

It is therefore respectfully submitted that the Examiner's comments are not supported by the disclosure of the Reesor et al. patent.

In view of the foregoing amendment and remarks, it is respectfully submitted that claims 1–8 are in condition for allowance and a Notice to that effect is respectfully requested.

Respectfully submitted,



Paul F. Wille
Reg. No. 25,274
Attorney for Applicant

6407 East Clinton Street
Scottsdale, AZ 85254
tel.: 602 549–9088
fax.: 480 778–0304

VERSION WITH MARKINGS TO SHOW CHANGES

In the description:

Please change the paragraph beginning at page 2, line 31, to read as follows.

Typically, these systems are implemented in digital form and manipulate large amounts of data in analyzing the input signals. The Sacca patent discloses an analog system using an amplifier with hysteresis to avoid dithering, which, to a large extent, is unavoidable with a simple amplitude comparison. On the other hand, an extensive computational analysis to determine relative power takes too long. The Eryilmaz patent attempts to simplify the amount of computation but still requires manipulation of significant amounts of data. [In all] All these systems manipulate amplitude data, or data derived from amplitude, up to the point of making a binary value signal indicating receive or transmit.

The paragraph beginning at page 5, line 9, is changed as follows.

– – In accordance with the invention, register 10 is incremented or decremented depending upon a three bit word representing the states of the signals on the microphone input and the line input to a telephone (not shown in FIG. 1). The direction of the count is determined by whether or not the signal on the microphone input is larger than the signal on the line input. Thus, entering region 11 implies a relatively consistent signal on the microphone input and entering region 16 implies a relatively consistent signal on the line input. The size of a region defines how much variation is tolerated before one exits the region. The regions need not [by] be symmetrical about zero. Thus, moving threshold 13 further away from zero than threshold 17 biases the system to favor the line input. Similarly, making region 11 smaller than region 16 biases the system to favor the line input. Register 10 accumulates data for a period of time defined as a window. Data in a window and in successive windows contribute to the decision on whether to receive or transmit. – –

The paragraph beginning at page 5, line 27, is changed as follows.

Comparator 25 is coupled to the outputs of amplifiers 23 and 24 and provides [and] an indication of which signal is the larger. Comparator 26 compares the

rectified line input signal to a threshold value and provides a signal indicating which is larger. Comparator 27 compares the rectified microphone input signal to another threshold value and provides a signal indicating which is larger. The outputs of comparators 25, 26, and 27 are coupled to D-flip-flops 31, 32, and 33, which latch the data on each clock pulse, e.g. on line 34 to D-flip-flop 33. In one embodiment of the invention, the input signals are sampled at 44.1 kHz. Other sampling rates could be used instead.

The paragraph beginning at page 7, line 10, is changed as follows.

FIG. 4 is a schematic of a signal analyzer constructed in accordance with a preferred embodiment of the invention. Input 61 is coupled to the output of D-flip-flop 31 (FIG. [1] 2), input 62 is coupled to the output of D-flip-flop 32 (FIG. [1] 2), and input 63 is coupled to the output of D-flip-flop 33 (FIG. [1] 2). Inputs 61 and 62 are coupled to AND gate 65, which produces a logic "1" when the received signal (line input) is greater than the microphone signal and is greater than a predetermined threshold. The output of AND gate 65 is coupled to the "down" input of accumulator 40. Inverted input 62 and input 63 are coupled to AND gate 66, which produces a logic "1" when the received signal (line input) is less than a predetermined threshold and the microphone signal is greater than a predetermined threshold. The thresholds need not be the same value. The output of AND gate 66 is coupled to the "up" input of accumulator 40.

In the claims:

Claims 1 and 2 have been amended as follows.

1 (Amended). A method for comparing two electrical signals, said method comprising the steps of:

(a) comparing the signals to each other and to at least one threshold to produce [samples representative] a binary representation of the comparisons [signals];

(b) converting a plurality of [samples] binary representations into a first count; and

(c) comparing the first count to at least one count threshold.

sub B cont'd

2 (Amended). The method as set forth in claim 1 wherein comparing step (a) includes the steps of:

comparing the signals in an analog comparator;

sampling the output of the comparator to produce [a] said binary representation of the comparison.